The Document is Applied to: CS9370DGP、CS9370DGO

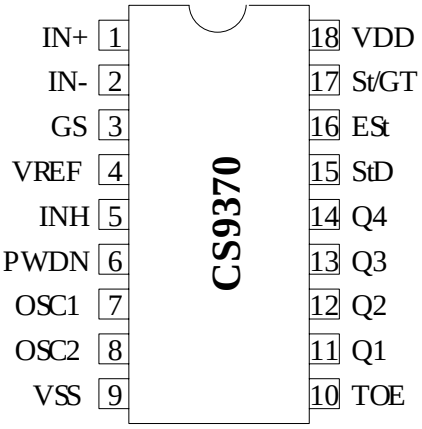
General Description

The CS9370 is a complete DTMF receiver integrating both the bandsplit filter and digital decoder functions. The filter section uses switched capacitor techniques for high-and low-group filters and dial-tone rejection. Digital counting techniques are employed in the decoder to detect and decode all 16 DTMF tone-pairs into 4-bit code. External component count is minimized by on-chip provision of a differential input amplifier, clock-oscillator and latched 3-state bus interface.

Features

- CMOS, 5/3 Volt operation.
- Excellent performance with minimum board quality.
- Central office quality.
- Low power consumption.
- Power-Down mode
- Inhibit-mode
- Package: DIP18, SOP18

Pin Configuration



Absolute Maximum Ratings

Supply Voltage: .....-0.3 ~ +6.0V
Operating Temperature: .....-40 ~ +85℃
Storage Temperature: .....-65 ~ +150℃
Power Dissipation: 35mW

DC Electrical Characteristics (Unless otherwise specified: Ta=25℃)

Parameter	*Description*	*Test Condition*	*Min.*	*Typ.*	*Max.*	*Unit*
SUPPLY:						
V_{DD}	Operating supply voltage		2.5		5.5	V
I_{CC}	Operating supply current			3.0	7	mA
P_O	Power consumption	F=3.579MHz; V_{DD}=5V		15	35	mW
I_S	Standby current	$V_{PWDN}=V_{DD}$			100	μA
INPUTS:						
V_{IL}	Low level input voltage				1.5	V
V_{IH}	High level input voltage		3.5			V
I_{IH}/I_{IL}	Input leakage current	$V_{IN}=V_{SS}$ or V_{DD}		0.1		μA
I_{SO}	Pull up (source) current	TOE（Pin 10）=0V		7.5	15	μA
R_{IN}	Input Signal Impedance (Inputs 1, 2)	@1kHz		10		MΩ
V_{TST}	Steering threshold voltage			2.35		V
OUTPUT:						
V_{OL}	Low level output voltage	No load		0.03		V
V_{OH}	High level output voltage	No load		4.97		V
I_{OL}	Output low (sink) current	V_{OUT}=0.4V	1.0	2.5		mA
I_{OH}	Output High (source) current	V_{OUT}=4.6V	0.4	0.8		mA
V_{REF}	Output voltage	No load	2.4		2.7	V
R_{OR}	Output resistance			10		kΩ

Operating Characteristics

Gain Setting Amplifier

Parameter	Description	Test Condition	Typ.	Unit
I_{IN}	Input leakage current	$V_{SS}<V_{IN}<V_{DD}$	± 100	nA
R_{IN}	Input resistance		10	MΩ
V_{OS}	Input offset voltage		± 25	mV
PSRR	Power supply rejection	1kHz	60	dB
CMRR	Common mode rejection	$-3.0<V_{IN}<3.0$	60	dB
A_{VOL}	DC open loop voltage gain		65	dB
F_C	Open loop unity gain bandwidth		1.5	MHz
V_D	Output voltage swing	$R_L \geqslant 100k\Omega$ to V_{SS}	4.5	V_{PP}
C_L	Tolerable capacitive load (GS)		100	pF
R_L	Tolerable resistive load (GS)		50	kΩ
V_{CM}	Common mode range	No load	3.0	V_{PP}

AC Characteristics

Parameter	Description		Min.	Typ.	Max.	Unit	Note
	Valid input signal level (each tone signal)	Min			-40	dBm	1,2,3,5,6,9,11
					7.75	mV_{RMS}	1,2,3,5,6,9,11
		Max	+1			dBm	1,2,3,5,6,9,11
			883			mV_{RMS}	1,2,3,5,6,9,11
	Twist accept limit	Positive		10		dB	2,3,6,9,11
		Negative		10		dB	
	Freq. deviation accept limit			± 1.5% ± 2Hz		Nom.	2,3,5,9,11
	Freq. deviation reject limit		± 3.5%			Nom.	2,3,5,11
	Third tone tolerance			-16			2,3,4,5,9,10,11
	Noise tolerance			-12		dB	2,3,4,5,7,9,10,11
	Dial tone tolerance			+18		dB	2,3,4,5,8,9,10,11
TIMING:							
t_{DP}	Tone present detection time		5	14	16	ms	
t_{DA}	Tone absent detection time		0.5	4	8.5	ms	
t_{REC}	Tone duration accept				40	ms	
t_{REC}	Tone duration reject		20			ms	(User adjustable)
t_{ID}	Interdigit pause accept				40	ms	(User adjustable)
t_{DO}	Interdigit pause reject		20			ms	(User adjustable)
OUTPUTS:							
t_{PQ}	Propagation delay (St to Q)			8	11	µs	TOE=V_{DD}
t_{PSED}	Propagation delay (St to StD)			12		µs	
t_{QSED}	Output data se up (Q to Std)			4.5		µs	
t_{PTE}	Propagation ENABLE			50	60	ns	R_L=10kΩ
t_{PTD}	Delay (TOE to Q) DISABLE			300		ns	C_L=50pf
CLOCK:							
f_{CLK}	Crystal/Clock frequency		3.5759	3.5795	3.581	MHz	
C_{LO}	Clock output (OSC2) Capacitive Load				30	pf	

Notes:

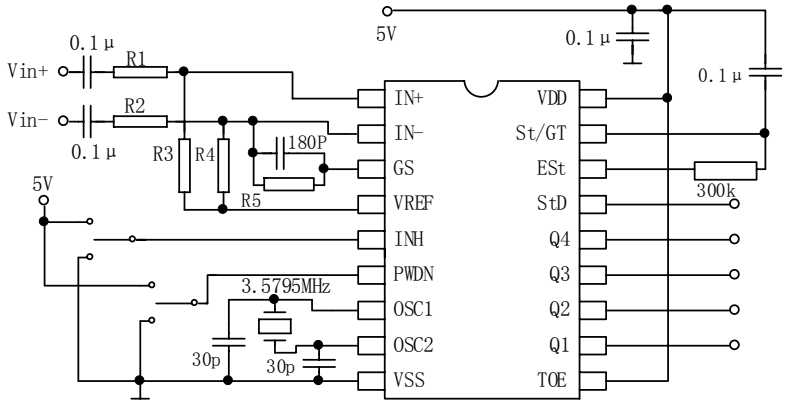
1. dBm = decibels above or below a reference power of 1mW into a 600Ω load.
2. Digit sequences consist of all 16 DTMF tones.
3. Tone duration = 40ms, Tone pause = 40ms
4. Nominal DTMF frequencies are used.
5. Both tones in the composite signal have an equal amplitude.
6. Tone pair is deviated by ± 1.5% ± 2Hz.

7. Bandwidth limited (3kHz) Gaussian Noise.
8. The precise dial tone frequencies are (350Hz and 440Hz) ± 2%.
9. For an error rate of less than 1 in 10,000.
10. Reference to the lowest level frequency component in DTMF signal.
11. Added a 0.1μf capacitor between V_{DD} and V_{SS}.

Pin Description

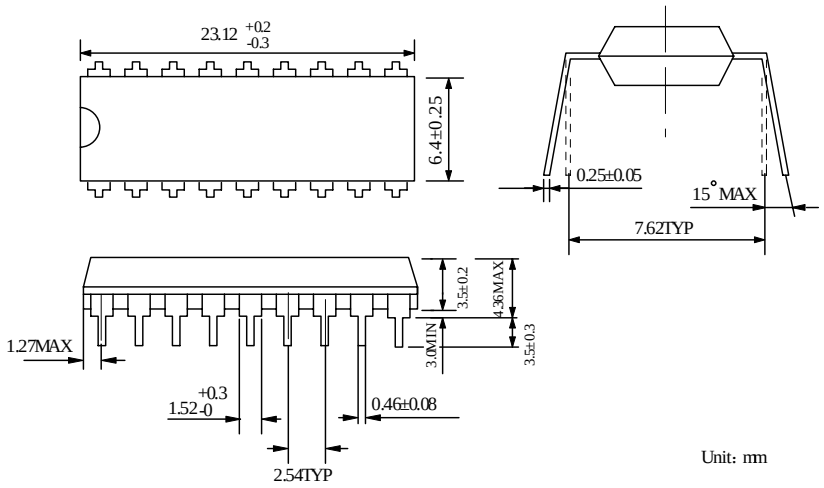
Pin	Sym.	I/O	Port	Function
1	IN+	I	-	Non-Inverting input. Connections to the front-end differential amplifier.
2	IN-	I	-	Inverting input. Connections to the front-end differential amplifier.
3	GS	O	-	Gain select. Gives access to output of front-end differential amplifier for connection of feedback resistor.
4	VREE	O	-	Reference voltage output, nominally VDD/2. May be used to bias the inputs at midair.
5	INH	I	CMOS IN pull down	Inhibit (input) logic high inhibit the detection of 1633Hz internal built-in pull down resistor.
6	PWDN	I	CMOS IN pull down	Power down (input). Active high power down the device and inhibit the oscillator internal built-in pull down resistor.
7	OSC1	I	-	Clock Input — 3.579545MHz crystal connected between these pins completes internal oscillator or ceramics generator.
8	OSC2	O	-	Clock Output
9	VSS		-	Negative power supply, normally connected to 0V.
10	TOE	I	CMOS IN pull up	3-state data output enable (input). Logic high enables the outputs Q1 ~ Q4.
11 ~ 14	Q1 ~ Q4	O	-	3-state data outputs. When enabled by TOE, provide the code corresponding to the last valid tone-pair received.
15	StD	O	CMOS OUT	Delayed steering output. Presents a logic high when the voltage on St/GT falls below V_{TSt}.
16	Est	O	CMOS OUT	Early steering output. Presents a logic high immediately when the digital algorithm detects a recognizable tone-pair (signal condition). Any momentary loss of signal condition will cause Est to return to a logic low.
17	St/GT	I/O	CMOS I/O	Steering input/guard time output (bi-directional). A voltage greater than V_{TSt} detected as St causes the device to register the detected tone-pair and update the output latch. A voltage less than V_{TSt} free the device to accept a new tone-pair. The GT output acts to reset the external steering time-constant; its state is a function of Est and the voltage on St.
18	VDD		-	Positive power supply.

Application Circuit (for Reference only)



Pin Dimensions

DIP18



SOP18